

CLAIMS

1. An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with a first layer and a second mark portion associated with a second layer, wherein each mark portion comprises a single two dimensional generally orthogonal array of individual test structures.
2. An overlay metrology mark in accordance with claim 1 wherein each mark portion is developed within or on the said layer.
3. An overlay metrology mark in accordance with claim 2 wherein each mark portion is printed on the said layer by a microlithographic process.
4. An overlay metrology mark in accordance with any preceding claim wherein each mark portion comprises a single two dimensional generally substantially square array of individual test structures with generally constant spacing between test structures throughout the array.
5. An overlay metrology mark in accordance with any preceding claim wherein the spacing between test structures in the array comprising the first mark portion and the spacing between test structures in the array comprising the second mark portion is equivalent.
6. An overlay metrology mark in accordance with any preceding claim wherein each mark portion has a generally square overall outline.
7. An overlay metrology mark in accordance with any preceding claim wherein each test structure has a width of around 0.5 to 2 μm .

8. An overlay metrology mark in accordance with any preceding claim wherein spacing between test structures in the array is between one and four structure widths.
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9. An overlay metrology mark in accordance with any preceding claim wherein the individual test structures making up each array are substantially identically sized and shaped and have generally square geometry.
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10. An overlay metrology mark in accordance with any preceding claim wherein the individual test structures comprise arrangements of design rule sized sub-structures.
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11. An overlay metrology mark in accordance with claim 10 wherein the arrangements of design rule sized sub-structures are selected from parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array, arrays of holes within a suitably shaped test structure and any
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- combinations of these or other like patterns.
12. An overlay metrology mark in accordance with claim 10 or 11 wherein sub-structures are of design rule dimensions.
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13. An overlay metrology mark in accordance with any preceding claim wherein the arrays of test structures making up the first and second mark portions are disposed such that the first portion overlays the second portion and that the test structures of second portion are arrayed within the gaps between the test structures of the first portion and visible
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- therebetween.

14. An overlay metrology mark in accordance with claim 13 wherein each test structure in the second portion is located at the diagonal centre of a square bounded at each corner by test structures of the first portion.
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15. An overlay metrology mark in accordance with any one of claims 1 to 12 wherein the test structures making up the first and second mark portions are disposed such that the first portion is laterally spaced from the second portion in a spacing direction parallel to a horizontal or vertical direction of the square arrays such that a notional line in the spacing direction can be drawn about which each array exhibits mirror symmetry.
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16. An overlay metrology mark in accordance with claim 15 wherein each mark portion comprises an identical pattern of test structures.
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17. A method for providing an overlay metrology mark to determine the relative position between two or more layers of an integrated circuit structure comprises the steps of:
- laying down a first mark portion in association with a first layer;
- 20 and laying down a second mark portion in association with a second layer;
- wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures.
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18. A method for determining the relative position between two or more layers of an integrated circuit structure comprises the steps of:
- laying down a first mark portion in association with a first layer;
- laying down a second mark portion in association with a second layer;
- wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures;
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optically imaging the two mark portions;
collecting and digitizing the image;
numerically analysing the digitized data to obtain a quantified
measurement of the misalignment of the first and second mark portions.

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19. The method of claim 18 wherein optical imaging of the mark is carried
out using bright field microscopy.

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20. The method of one of claims 17 to 19 wherein each mark portion is
developed within or on the said layer.

21. The method of one of claims 17 to 20 wherein each mark portion is laid
down by a microlithographic process.

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22. A mark or method substantially as hereinbefore described with reference
to the accompanying drawings.